Amendments to the Claims

Claims 1-10 (Canceled).

11. (Currently Amended): Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising a semiconductive silicon comprising layer of silicon-on-insulator circuitry, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

an insulator layer of the silicon-on-insulator circuitry received on the silicon comprising layer, the insulator layer comprising a first silicon dioxide comprising region in contact with the silicon comprising layer and running along ~~at least~~ only a portion of the channel region between the source/drain regions, a silicon nitride comprising region in contact with the first silicon dioxide comprising region and running along at least a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon nitride comprising region, the silicon nitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

Claims 12 and 13 (Canceled).

14. (Original): The circuitry of claim 11 wherein the silicon nitride comprising region has a thickness of from about 10 Angstroms to about 50 Angstroms.

15. (Original): The circuitry of claim 11 wherein the first silicon dioxide comprising region has a thickness of from about 10 Angstroms to about 30 Angstroms.

16. (Original): The circuitry of claim 11 wherein the source/drain regions extend to the insulator layer.

Claim 17-61 (Canceled).

62. (New) Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising a semiconductive silicon comprising layer of silicon-on-insulator circuitry, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

an insulator layer of the silicon-on-insulator circuitry received on the silicon comprising layer, the insulator layer comprising a first silicon dioxide comprising region in contact with the silicon comprising layer and running along only a portion of the channel region between the source/drain regions, a silicon oxynitride comprising region in contact with the first silicon dioxide comprising region and running along at least a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon oxynitride comprising region, the silicon oxynitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

63. (New): The circuitry of claim 62 wherein the silicon oxynitride comprising region has a thickness of from about 10 Angstroms to about 50 Angstroms.

64. (New): The circuitry of claim 62 wherein the first silicon dioxide comprising region has a thickness of from about 10 Angstroms to about 30 Angstroms.

65. (New): The circuitry of claim 62 wherein the source/drain regions extend to the insulator layer.

65. (New): The circuitry of claim 62 wherein the silicon comprising layer has a thickness from about 1000 Angstroms to about 2000 Angstroms.

66. (New): The circuitry of claim 11 wherein the silicon comprising layer has a thickness from about 1000 Angstroms to about 2000 Angstroms.